

FIG. 1

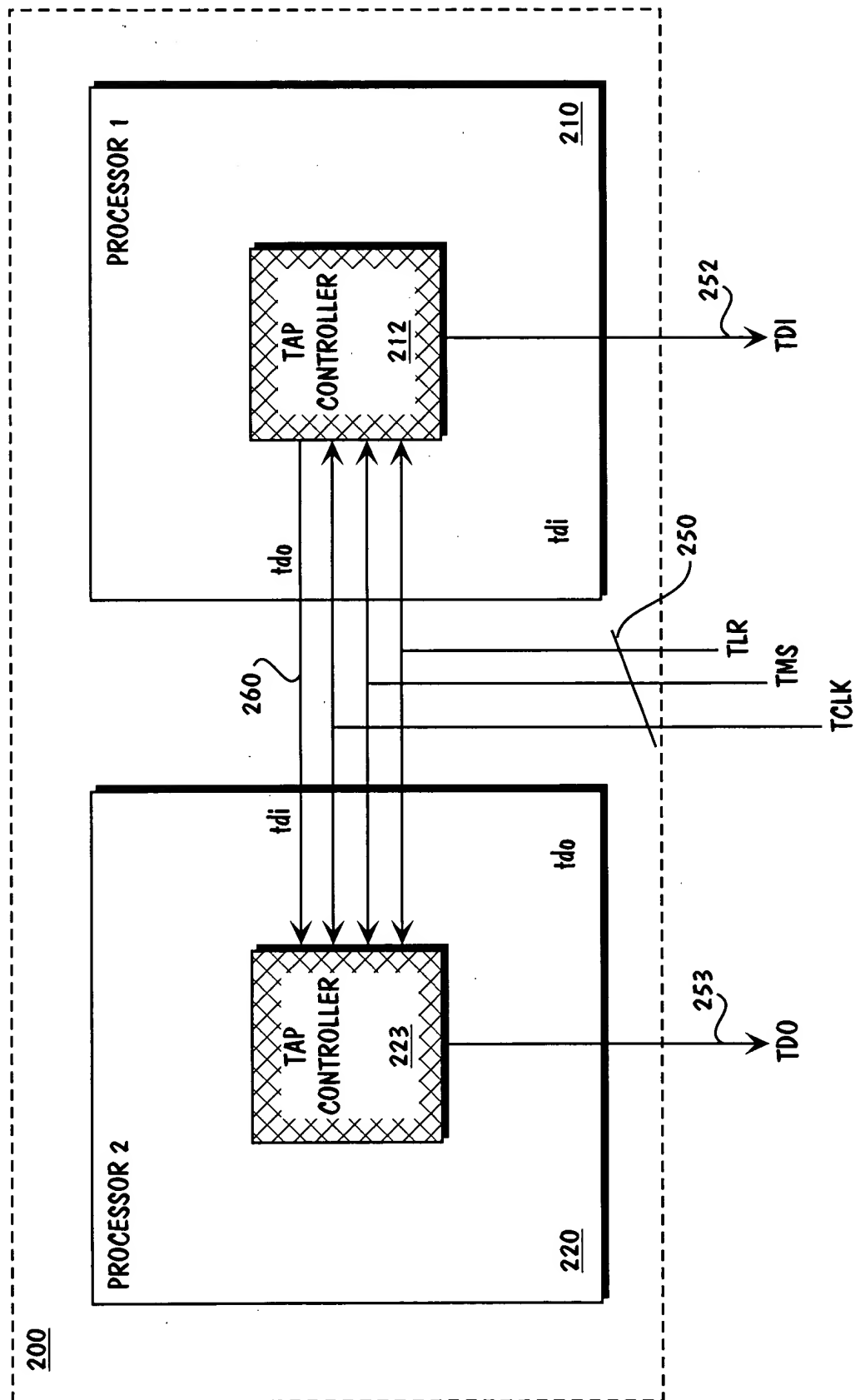


FIG. 2

FIG. 3a

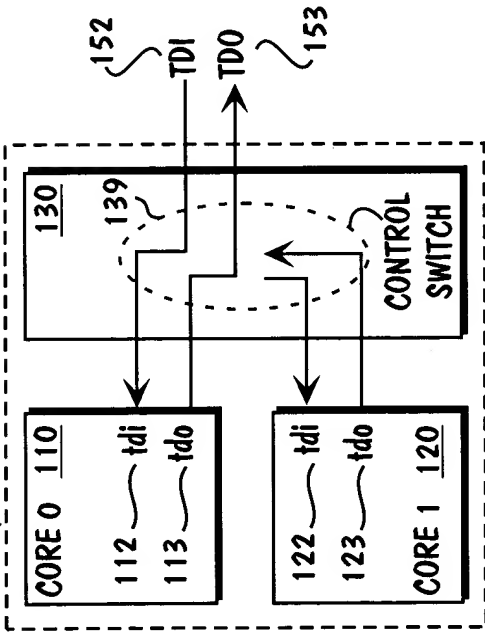


FIG. 3b

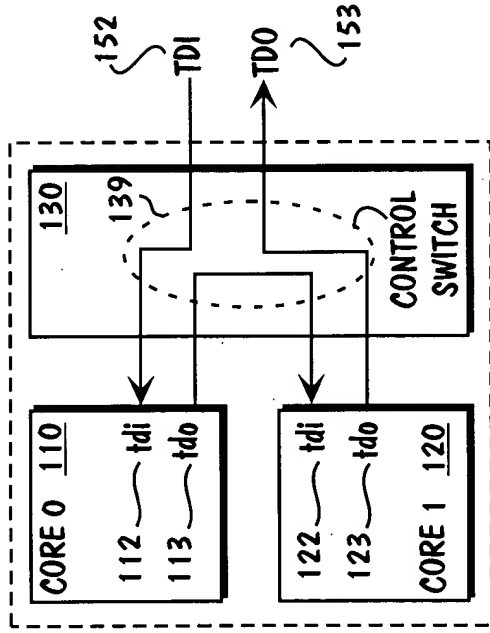
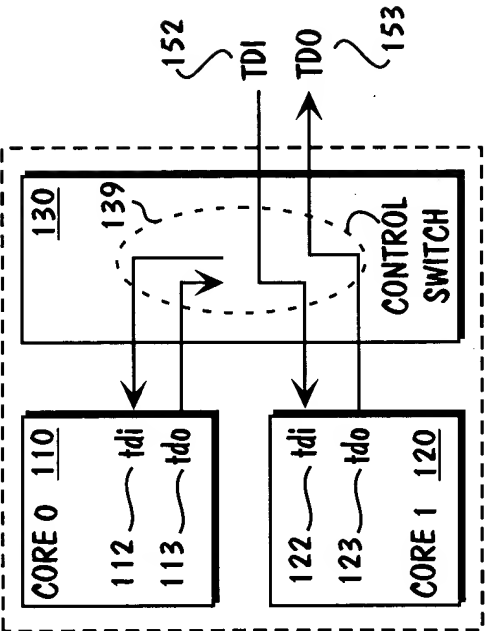


FIG. 3c

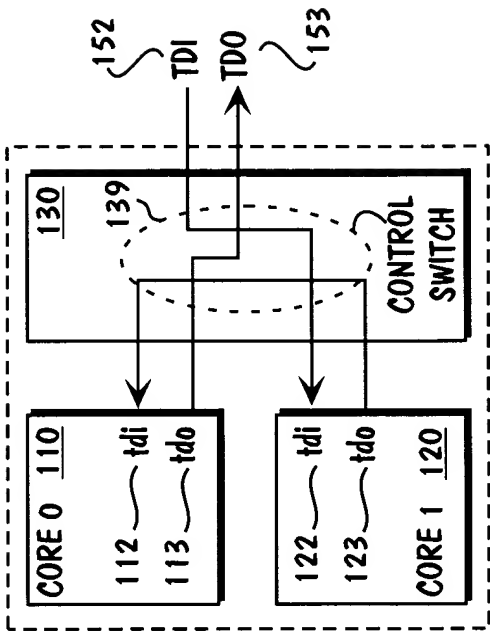


FIG. 3d

FIG. 4a

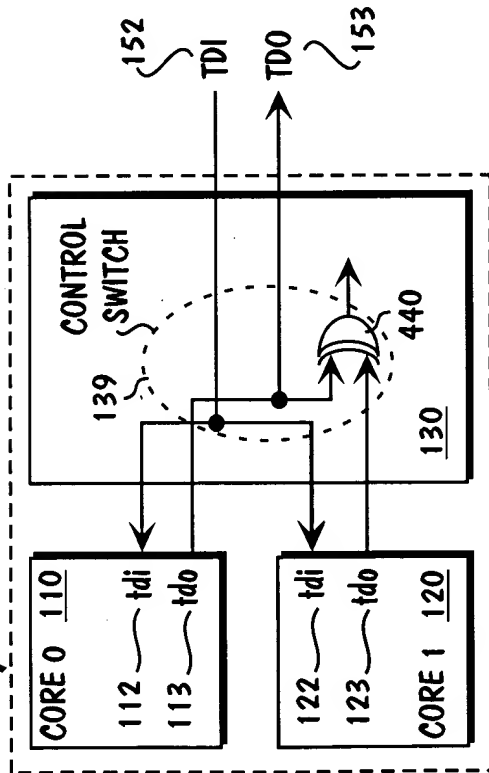


FIG. 4b

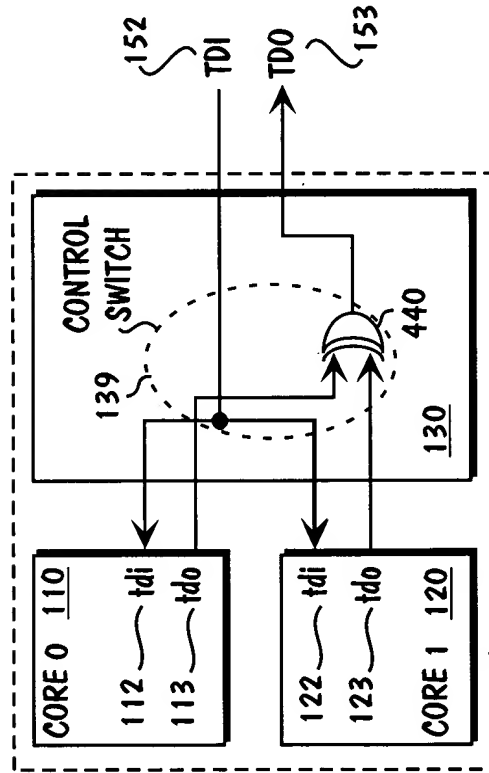
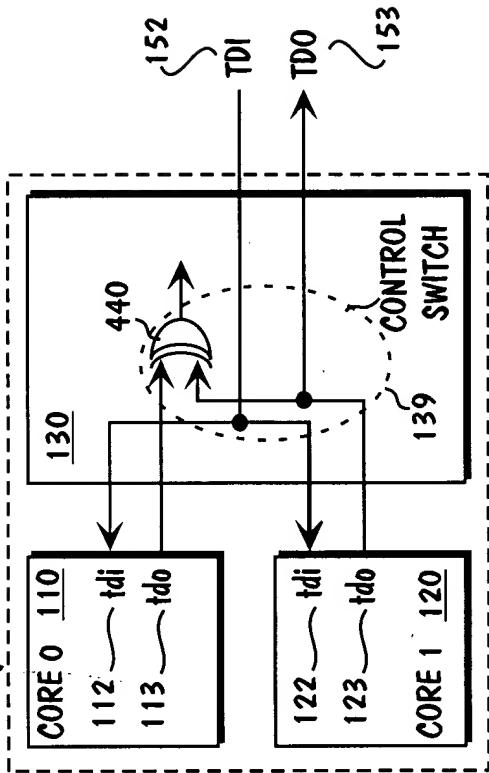


FIG. 4c

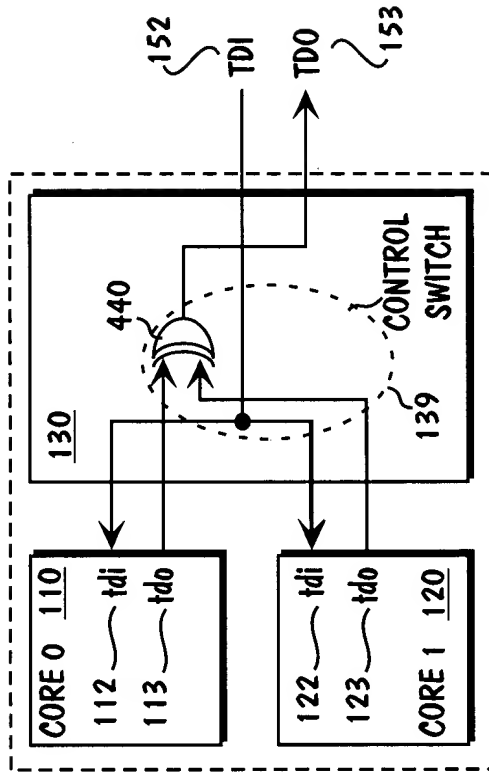


FIG. 4d



# INTEGRATED TEST BUS

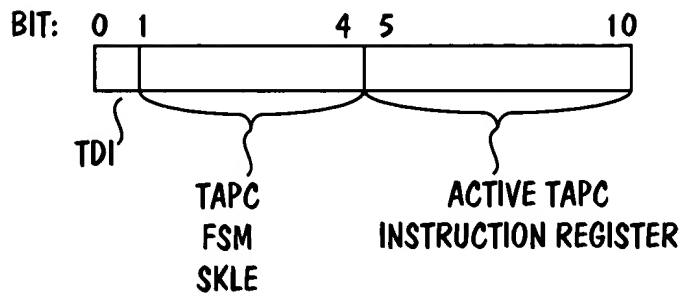


FIG. 6

# TAP CORE CONFIGURATION REGISTER

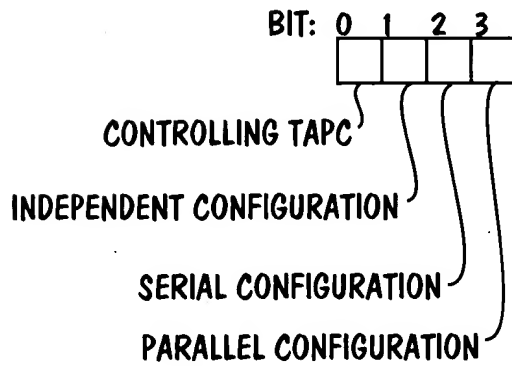


FIG. 7

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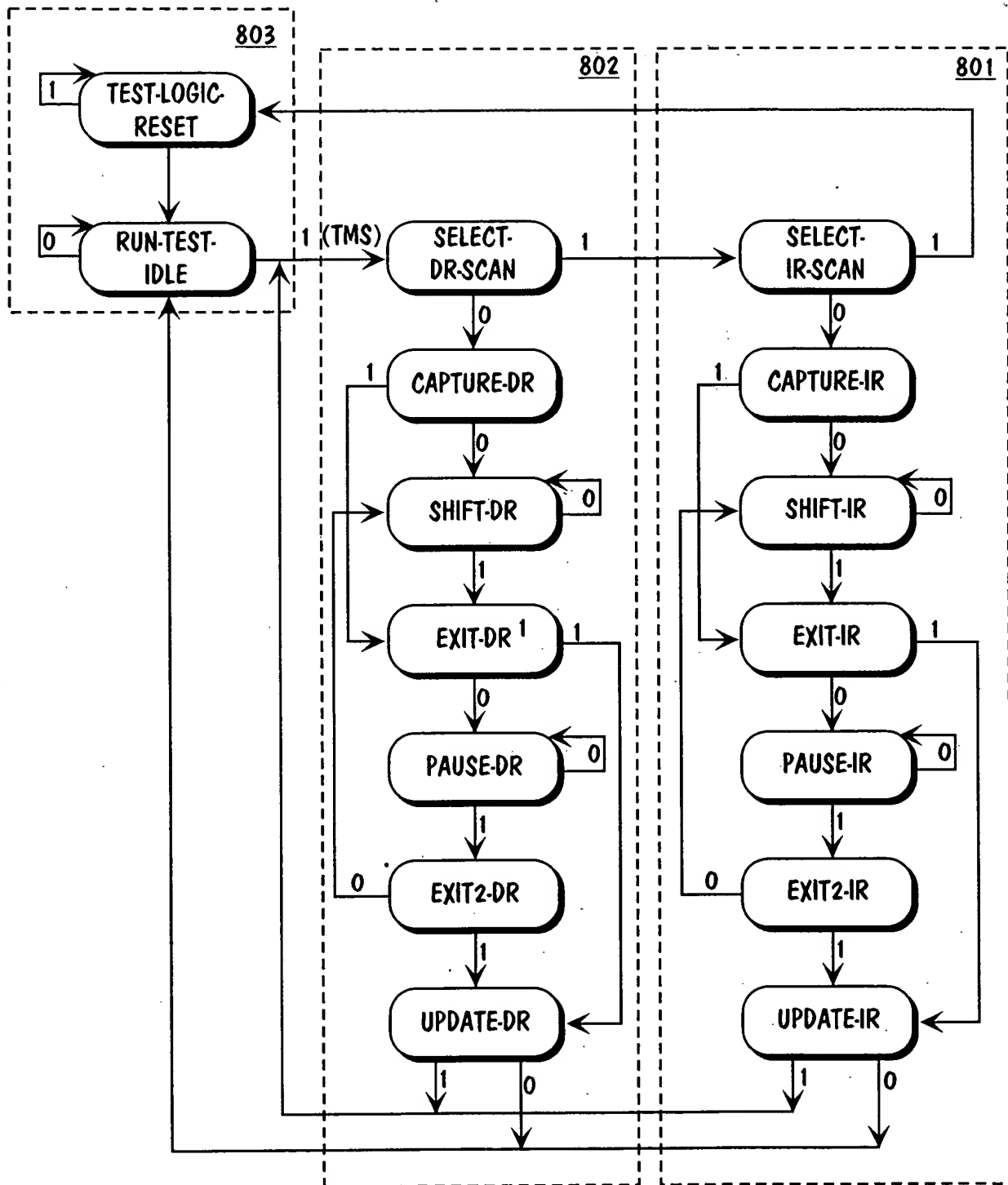


FIG. 8

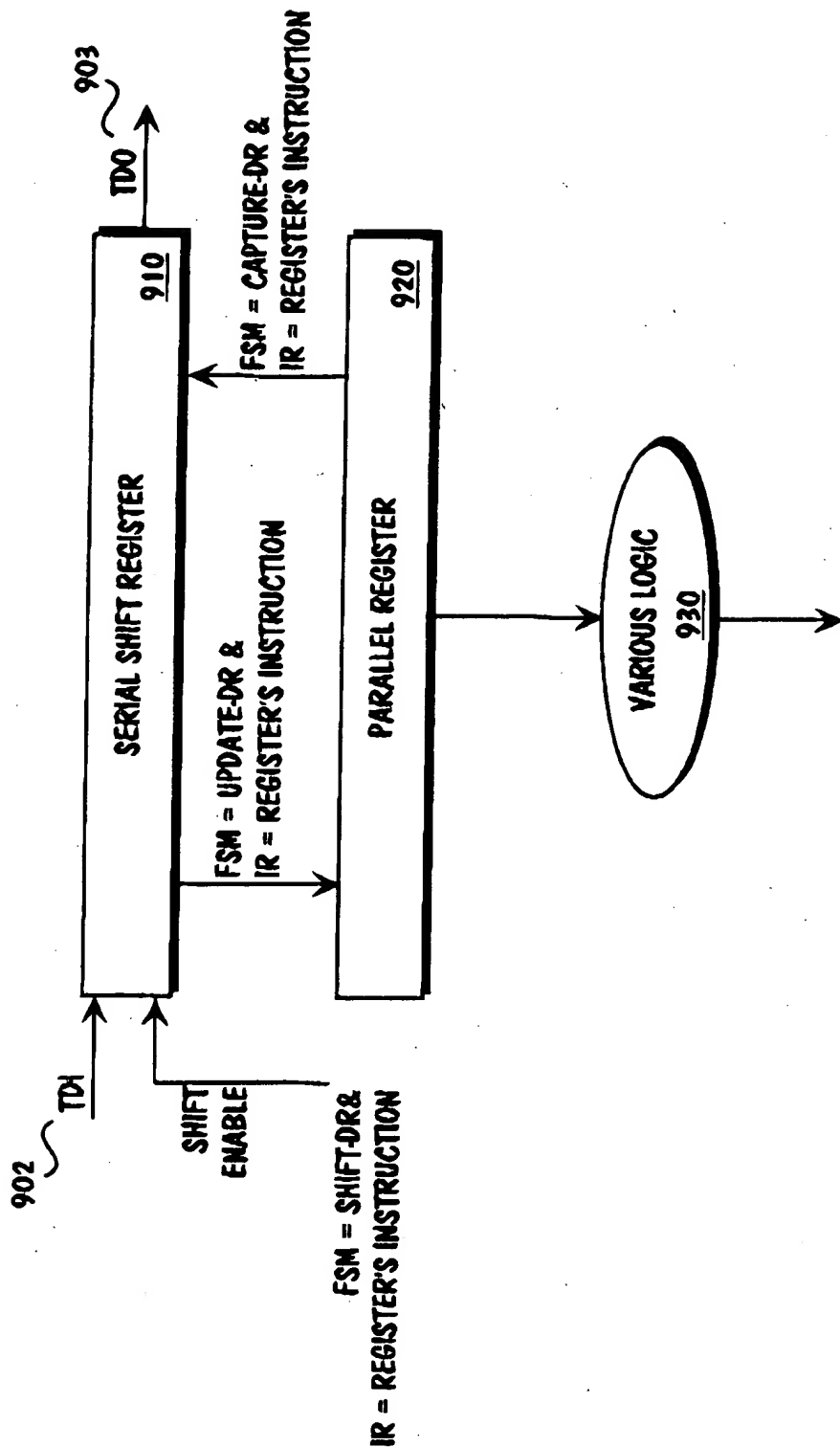


FIG. 9